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Letter

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Interface Passivation and Trap Reduction via a Solution-Based Method for Near-Zero Hysteresis Nanowire Field-Effect Transistors

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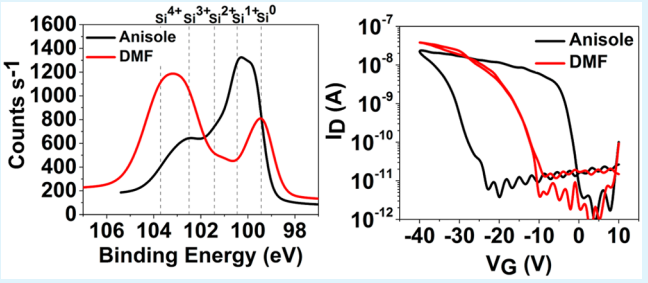
Supporting Information

ABSTRACT: In this letter, we demonstrate a solution-based method for a one-step deposition and surface passivation of the as-grown silicon nanowires (Si NWs). Using *N*,*N*-dimethylformamide (DMF) as a mild oxidizing agent, the NWs' surface traps density was reduced by over 2 orders of magnitude from 1×10^{13} cm^{-2} in pristine NWs to 3.7×10^{10} cm^{-2} in DMF-treated NWs, leading to a dramatic hysteresis reduction in NW field-effect transistors (FETs) from up to 32 V to a near-zero hysteresis. The change of the polyphenylsilane NW shell stoichiometric composition was confirmed by X-ray photoelectron spectroscopy analysis showing a 35% increase in fully oxidized Si^{4+} species for DMF-treated NWs compared to dry NW powder. Additionally, a shell oxidation effect induced by DMF resulted is a more stable NW FET performance with steady transistor currents and only 1.5 V hysteresis after 1000 h of air exposure.



KEYWORDS: *hysteresis, silicon nanowires, field-effect transistor, nanowire interface, DMF, XPS, interface trap reduction, interface passivation*

Silicon nanowires (Si NWs) are attractive candidates for building novel electronic devices using "bottom-up" solvent-based processing. Their unique physical and electrical properties, including single-crystal lattice structure, efficient charge-transport capabilities, and excellent mechanical flexibility,[1] attracted considerable research attention for the fabrication of chemical and biological sensors,[2−4] high-performance field-effect transistors (FETs),[5−7] and optical devices.[7] Leiber's group has demonstrated a charge mobility of 1350 cm^2 V^{-1} s^{-1} using boron-doped chemical vapor deposition (CVD)-grown Si NWs as semiconducting materials in the FETs, emphasizing the potential for high-mobility devices.[5] Oriented Si NWs can be printed and solution-processed on electrode structures on flexible substrates using various deposition techniques,[1] suitable for the production of electronic devices on a roll-to-roll basis for industrial applications. This highlights their compatibility with low-temperature processing steps for plastic and printed electronic device applications such as artificial e-skin[8] and chemical sensors.[9]

To enable truly large area printed electric devices incorporating semiconducting nanowires (NWs), a scalable NW growth technology is required. CVD-based growth methods struggle to deliver significant amounts of NW powder because of limited substrate size and the high cost of growth processes. On the contrary, a supercritical fluid−liquid−solid (SFLS) method[10] has the ability to tune the NW synthesis and to be scaled-up for kilogram per day production, suitable for industrial applications.[11] However, the SFLS-grown Si NWs are covered with an amorphous polyphenylsilane shell during the synthesis. The shell is mostly composed of carbon, oxygen, and silicon species, as we discuss later, with silicon being in various oxidation states (Si^+, Si^{2+}, Si^{3+}, and Si^{4+}), contributing to the NW surface states that play an important role in the electronic properties, and can dramatically affect the NW device performance such as in FETs. Trapping of the charge carriers at the semiconductor/dielectric interface, including the NW shell region, can lead to a hysteresis effect in devices I−V characteristics and low charge mobility.

Hysteresis in the NW, carbon nanotube, and organic-based FETs, especially utilizing SiO_2 dielectrics, is the main source for performance instabilities that affect the reproducibility and reliability of the devices. Hysteresis represents a shift in the threshold voltage (V_{th}) under the application of gate bias.

The hysteresis behavior mainly originates from electron and hole trapping/detrapping at the semiconductor/insulator

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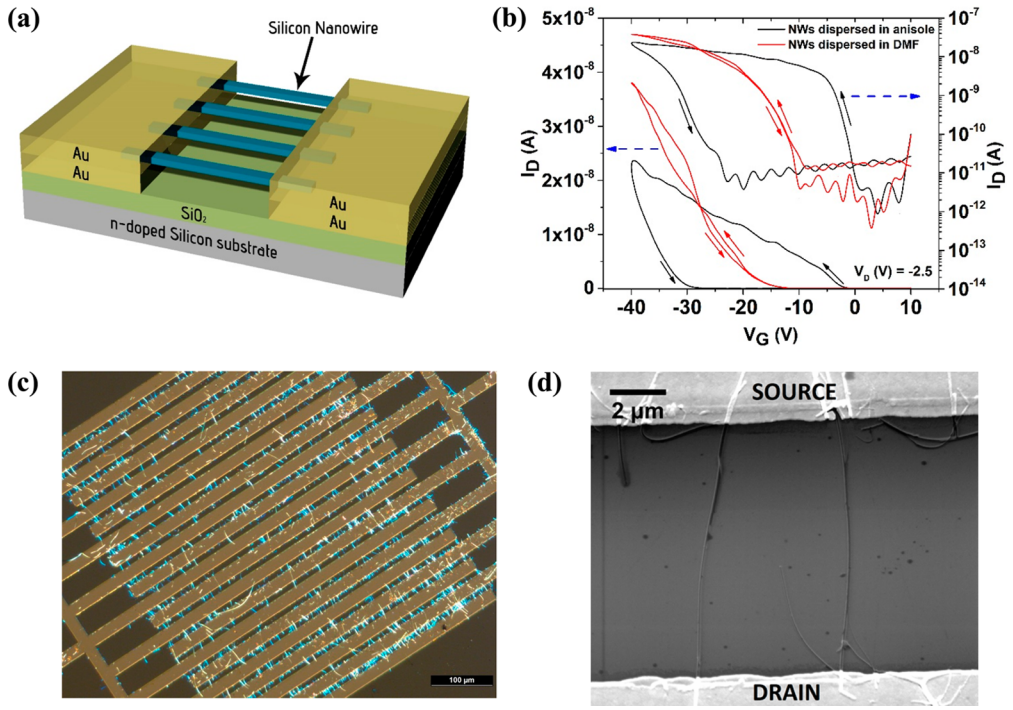

Figure 1. (a) Schematic diagram of the FET device showing the NWs aligned across the channel area and the double-layer gold ohmic contacts, where a doped silicon substrate serves as the common gate electrode. (b) Transfer characteristics of the bottom-gated Si NW FET shown in linear and log-linear scales. The arrows show the direction of the gate voltage scan. A high hysteresis of 30 V (black line) was exhibited when NWs are dispersed in anisole and a very low hysteresis of 0.9 V when NWs are dispersed in DMF (red line) because of significant reduction of the hole traps. POM (c) and SEM (d) images of a typical FET device used in this work with Si NWs aligned across a 10 μm gap between gold electrodes.

interface due to dielectric surface functionalities and adsorbed small molecules (e.g., oxygen and water) by the silanol groups at the interfacial layer between the semiconducting material and the gate dielectric.[12] These silanol groups (Si−OH), also known as hydroxyl groups, can be formed at the silicon oxide surface even during the synthesis of silica[13] and not just through atmospheric exposure. A high density of water molecules at the SiO_2 surface was shown to induce a hysteresis exceeding 50% of the applied gate voltage in carbon nanotube FETs.[14] Additionally, hole trapping can originate from weak Si−Si bonds (excess silicon or oxygen vacancies) and weak Si−O bonds (siloxanes) near the Si/SiO_2 interface.[15]

In NW FETs, hysteresis can be observed in both moisture-free (dry glovebox) and ambient air conditions and is associated with strong bonding of polar water molecules to SiO_2 surfaces of NWs and substrates.

Annealing Si NWs at 700[16] and ∼1100 °C[17] in an oxygen environment was reported to form a SiO_2 passivation layer around the NWs, reducing the hysteresis caused by the surface states. Fukata et al.[18] demonstrated thermal oxidation using ozone to form a thick, good-quality SiO_2 layer on Si NWs at a lower temperature of 600 °C. However, such high-temperature annealing is not suitable for plastic electronic applications, and a low-temperature process is still required.

In this work, the hysteresis effect in solution-processed SFLS-grown Si NW FET devices was investigated, and a room-temperature solvent-based oxidizing-agent treatment was applied to demonstrate reproducible bottom-gated NW FETs with very low/near-zero hysteresis. The choice of solvents had a dramatic impact on the NW surface traps, and as shown for *N*,*N*-dimethylformamide (DMF), the trap density was reduced by over 2 orders of magnitude.

The undoped (intrinsic) Si NWs were grown via SFLS with monophenylsilane as a reactant in supercritical organic solvents.[10] The Si NWs have a single-crystal silicon core and an amorphous polyphenylsilane shell mainly composed of carbon (C 1s, 44%), oxygen (O 1s, 39%), and stoichiometric silicon (Si 2p, 15%), as verified by our X-ray photoelectron spectroscopy (XPS) analysis (Figure S2 and Table S1 in the Supporting Information, SI) and consistent with previous reports.[11] We used a bottom-gated FET configuration, where the NWs were deposited and aligned between device electrodes in a one-step process using dielectrophoretic self-alignment of NWs dispersed in a solvent with the application of an alternating electric field[19] (see the SI for the device's fabrication). The complete device structure is shown in Figure 1a. Over 15 solvents were investigated to produce dispersions of NWs, but only DMF and dimethylacetamide (DMA) have shown pronounced NW oxidation/passivation effects resulting in significant improvement of the NW transistor performance. For the studies presented in this paper, anisole was used as the reference solvent for NW dispersions. Parts c and d of Figure 1 show polarized optical microscopy (POM) and scanning electron microscopy (SEM) images of a typical Si NW FET device used in this work.

NW FETs were characterized using a Kiethley 4200 SCS semiconductor parameter analyzer in a dry N_2-filled glovebox to eliminate environmental effects causing degradation of the devices, and stability measurements were conducted in ambient air conditions. The change of the gate bias sweeping direction from forward to backward induced a shift in the threshold voltage, which was estimated for extraction of the hysteresis value (see the SI for NW hysteresis measurements).

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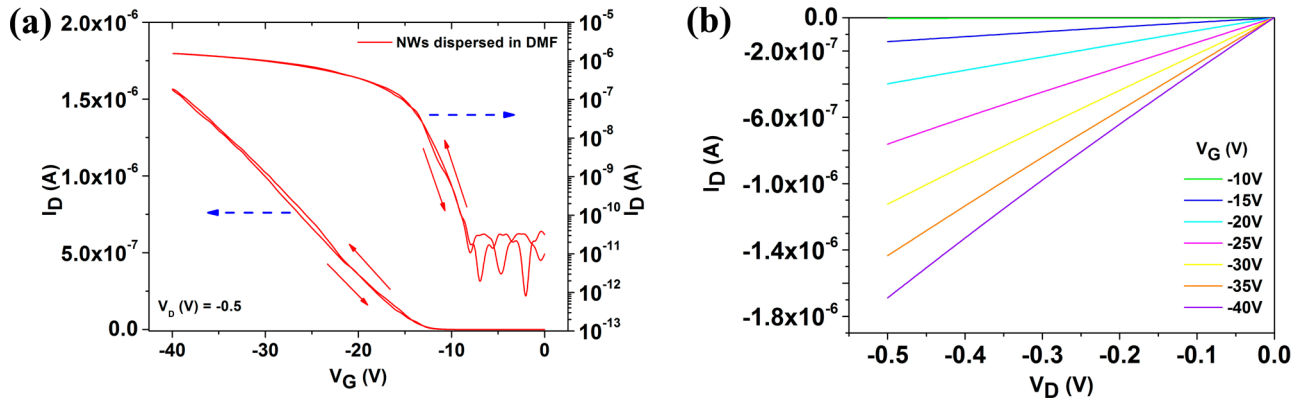

Figure 2. $I-V$ characteristics of DMF-treated Si NW FETs with 15 NWs in the channel. (a) Transfer characteristics obtained at $V_D = -0.5$ V showing a very low hysteresis of 0.1 V and a device mobility of 15 $cm^2 V^{-1} s^{-1}$ (eq 3). (b) Output characteristics showing an ohmic linear behavior of drain current versus drain voltage bias and also good gate modulation. V_G is increased in −5 V steps from −10 to −40 V.

The hysteresis values were obtained as the magnitude of the threshold voltage shift during the forward ($V_{th\_forward}$) and reverse ($V_{th\_reverse}$) sweeps of the gate voltage (V_G): $\Delta V_{th} = V_{th\_reverse} - V_{th\_forward}$. Hysteresis is associated with the traps through the relationship $\Delta V_{th} = \Delta Q_{trap}/C_i$,[20] where ΔQ_{trap} is the amount of trapped charge and C_i is the capacitance of the gate insulator.

The hysteresis values were extracted from the linear-regime FET transfer characteristics (Figure S1 in the SI).

Figure 1b demonstrates typical transfer characteristic data for Si NW FETs prepared using anisole and DMF as processing solvents. Anisole-processed NW FETs showed very large threshold voltage shifts for forward and reverse gate voltage scans, whereas DMF-processed devices demonstrated very small changes between the forward/reverse scans, and the transistor current at higher gate voltages (V_G = −25 to −40 V) was typically higher than the current in devices with anisole-dispersed NWs. The difference in hysteresis is significant and is attributed to the reaction of the dispersion solvent with the NW shell. Over 100 devices were fabricated and characterized during this work, and all of them showed the consistent trend where devices fabricated using DMF as a solvent exhibited a significant reduction in hysteresis compared to transistors fabricated with anisole. On the basis of a statistical analysis of 15 typical bottom-gated FET devices prepared with *each* solvent, the average hysteresis values (ΔV_{th}) of NWs dispersed in DMF and anisole were 3 and 25 V, respectively (Figure S3a and Table S2 in the SI).

The charge trap density (Q_{trap}) and the carrier mobility (μ) were estimated using the following equations:[6,21−23]

$$qQ_{trap} = \frac{C_{NW}|\Delta V_{th}|}{2\pi(Nr_{nw})L} \quad (1)$$

$$C_{NW} = N\frac{2\pi\varepsilon_0\varepsilon_r L}{\cosh^{-1}\left(\frac{r_{nw}+d}{r_{nw}}\right)} \quad (2)$$

$$\mu = \frac{L^2}{C_{NW}}\frac{1}{V_D}g_m \quad (3)$$

where q is the elementary charge, C_{NW} is the total gate capacitance based on the cylinder-on-plate model, which takes into consideration the electrostatic fringing effect,[6,22] ΔV_{th} is the hysteresis, N is the number of NWs crossing the FET channel, r_{nw} is the radius of the NW [~15 nm, transmission electron microscopy (TEM) results], L is the length of the NW in the FET channel (10 μm), ε_0 is the absolute permittivity, ε_r is the dielectric constant of the gate insulator (~3.9), and d is the thickness of the gate dielectric (~230 nm). In eq 3, g_m is the transconductance ($g_m = \partial I_D/\partial V_G$) and V_D is the applied source−drain voltage. Equation 1 was modified, taking into consideration the total number (N) of aligned NWs across the channel.

The density of occupied traps for the devices shown in Figure 1b was calculated using eqs 1 and 2. A Q_{trap} value of 1.2 × 10^{13} cm^{-2} was found for the anisole-treated NW FET, with ~120 NWs in the FET channel, whereas the trap density in the DMF-treated NW FET (with ~40 NWs) was 3.7 × 10^{11} cm^{-2}, demonstrating significant reduction of traps following DMF passivation. The results for one of the lowest trap densities, 3.7 × 10^{10} cm^{-2} achieved with DMF-dispersed NW FETs (Figure 2a,b), showed near-zero hysteresis of 0.1 V and ohmic output characteristics. Statistical analysis of over 30 NW FETs fabricated with anisole and DMF solvents demonstrated relatively widespread hysteresis values (ΔV_{th}) between 21 and 32 V corresponding to trap densities from 8.6 × 10^{12} to 1.3 × 10^{13} cm^{-2} for anisole-dispersed NWs (Figure S3a in the SI). On the contrary, the DMF-dispersed NW FETs showed significantly narrower hysteresis results between 0.1 and 5.1 V corresponding to Q_{trap} values from 3.7 × 10^{10} to 2.1 × 10^{12} cm^{-2} (Figure S3b in the SI).

The hysteresis effect was also investigated for NW devices exposed to ambient air for prolonged periods of time. ΔV_{th} was monitored for DMF-treated FETs for over 1000 h, and the hysteresis has steadily reduced from 8 to 1.5 V during this period (Figure S3c,e in the SI), indicating good channel passivation from ambient species including water molecules. Additionally, the transistor current marginally increased from 1.2 to 1.6 μA (Figure S3d in the SI). We speculate that residue of the DMF solvent still remains on the NW shell after DMF treatment of the FET device, and after exposure to air, it still contributes to mild oxidation and to the reduction of hysteresis over a longer period of time. This phenomenon is under further investigation.

An anisole-treated FET device, on the contrary, showed an increase of more than 10 V hysteresis in the initial 24 h period of exposure to air. However, the device current dropped five times during this short exposure, indicating degradation of the FET characteristics (Figure S4 in the SI).

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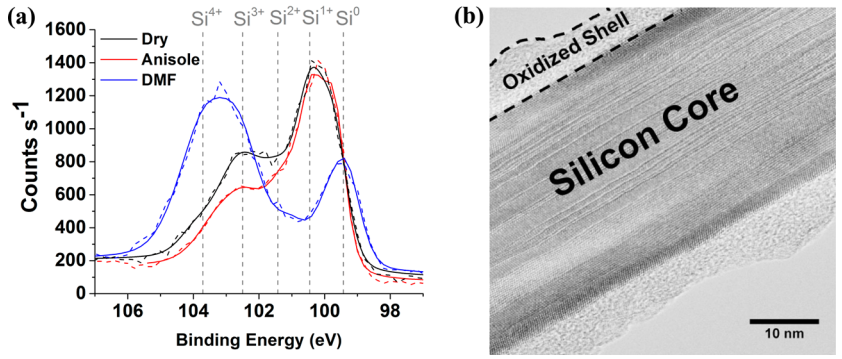

Figure 3. (a) High-resolution XPS spectrum of the Si 2p region of SFLS-grown Si NWs dispersed in anisole and DMF. The dashed lines indicate the different oxidation states of Si^0, Si^+, Si^{2+}, Si^{3+}, and Si^{4+}. After DMF treatment, the Si^{4+} peak increases significantly, while anisole treatment results in a small increase in the silicon peak compared to the dry sample. (b) High-resolution TEM (Hitachi HD-2300A STEM) image of Si NWs dispersed in DMF showing a single-crystal silicon core with 30 nm diameter and a ∼5−8-nm-thick amorphous oxidized polyphenylsilane shell.

Overall, the hysteresis behavior in our devices was consistent with previous reports for Si NW FETs, exhibiting an anticlockwise hysteresis when during the forward gate voltage scan the long-lived traps are populated with the majority of the carrier holes, and the FET threshold is then pushed to higher gate voltages, as exhibited by the reverse scan. The traps are considered to be located at the interfacial surface layer of the Si NW channel and the bottom-gated dielectric (SiO_2). The traps are mainly associated with the defects of the semiconducting nanomaterials, the dielectric surface functionalities, and the adsorbed water and oxygen molecules at/in the interfacial layers.[12] We speculated that DMF treatment is not likely to cause changes in the Si NW core structure, and the observed reduction of hysteresis is associated with the NW polyphenylsilane shell composition.

For investigation of the NW surface passivation, a high-resolution XPS technique was used to analyze the surface of the as-synthesized, DMF- and anisole-treated NWs (see the SI for NW characterization). Figure 3a illustrates the peak shapes of the Si 2p spectra of each sample, with the vertical lines showing the five different silicon subpeaks including the spin-splitting peak Si^0 (elemental silicon), the substoichiometric oxides Si^+ (Si_2O), Si^{2+} (SiO), and Si^{3+} (Si_2O_3), and the silicon dioxide peak Si^{4+} (SiO_2),[24] fitted using the Gaussian/Lorentzian function (Figure S5a−c in the SI), where the peak positions agree with the work of Bashouti et al.[25,26] By overlaying the peak line shapes, we observed a substantial difference in the oxidation states of the DMF-treated Si NW shell compared to the as-synthesized (dry) and anisole-treated Si NWs. Following DMF treatment, the main peak position of the Si 2p high-resolution XPS scan shifts from 100.3 (for dry silicon) and 100.1 (for anisole-treated silicon) to 103.2 eV, which corresponds to the formation of SiO_2 (Si^{4+}).[24]

In relation to the reference sample (dry NWs), the DMF treatment has the greatest impact on oxidation of the NW shells, showing a 35% increase in the SiO_2 peak (Si^{4+}) and further reduction of the other peaks, except the Si_2O_3 (Si^{3+}) peak, which stays relatively constant to the reference (Tables S3 and S4 in the SI). Also, the decrease in the silicon core (Si^0) peak (−8%) in the DMF-treated NWs suggests that the silica content has also increased compared with the anisole-treated NWs (Si^0 + 6%). Furthermore, the decrease in the Si^+ (−20%) and Si^{2+} (−5%) states indicates that the majority of the SiO_2 (Si^{4+}) increase comes from the early oxidization stages (Si^+ and Si^{2+}; Tables S3 and S4 in the SI).

Anisole-treated NWs, compared to the reference, show a slight decrease in Si^+ and Si^{3+}, with a slight increase in the Si^{2+} and Si^{4+} suboxide peaks (Tables S3 and S4 in the SI,). This result suggests that the treatment of the NWs using anisole either decreases the Si^+ and Si^{3+} oxides or etches the polyphenylsilane shell.

Overall, XPS analysis indicates that DMF treatment decreases the concentration of the Si^+ and Si^{2+} species and contributes to the increase of the SiO_2 (Si^{4+}) composition in the NW surface layer. Thus, the DMF solution acts as a mild chemical oxidizing agent for the polyphenylsilane shell.[27,28]

According to the C 1s XPS spectra, residues of anisole (Figure S6b in the SI) and DMF (Figure S6c in the SI) can be observed because of increases of the C−C and C═C signatures for anisole due to the presence of the aromatic ring and C═O in DMF.

Following XPS analysis, Si NWs were characterized by high-resolution TEM (Hitachi HD-2300A STEM). Figure 3b shows an image of a typical NW, with a 30-nm-diameter single-crystal core. During the NW growth, Si atoms diffuse into gold-seeded nanoparticles and are subsequently extruded, giving rise to a uniform core diameter along the NW, as set by the seed particle size. The light-gray layer around the silicon core indicates the presence of a 5−8-nm-thick oxidized amorphous shell. The increase of the silica amount (SiO_2) is likely to passivate the silicon core channel area, to provide stability against environmental aging, and to prevent the adsorption of water molecules that are responsible for the hysteretic behavior of the NW FET device. However, it is expected that the nonuniformity of the shell contributes to variations in the low hysteresis behavior of our devices. The shell's nonuniformity (∼35% variations in thickness) mainly originates from the local concentration gradients of polyphenylsilane byproducts that are randomly deposited along the NW core, resulting in a thicker shell at high concentrations and a thinner one at low concentrations. As a result, a distribution of the shell thickness both between the NWs and along a single NW is observed. Additionally, the oxide shell can act as a gate dielectric, providing an improvement in the interfacial properties between the Si NW core and the gate dielectric (SiO_2). Furthermore, because of the reduction of the trap states after DMF treatment and the corresponding increase of the transistor current (Figure 1b), the FET on/off current ratio between the "on" and "off" states is increased.

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We further investigated whether the passivation mechanism of DMF was applicable to NWs that have already been treated in anisole. Bottom-gated FETs were fabricated with NWs dispersed in anisole and then treated in DMF for a short period of time. The hysteresis reduced from 11 to 6 V when the FET device was dipped into DMF for 10 s, in ambient air (Figure S7a in the SI). An increase of the FET performance was also observed, with the output current (I_D) increasing from ∼0.95 to ∼4.3 μA (measured in a N_2-filled glovebox; Figure S7b in the SI) and an increase in the device mobility (μ) from 1 to 8 cm^2 V^{-1} s^{-1}. The reduction of the hysteresis indicates the fast formation of the oxide shell when the NWs are exposed to DMF, providing stability to the FET performance. Then, the device was exposed to ambient conditions for 1000 h, and the hysteresis only marginally increased by 0.6 V with a further increase in the device mobility to 9 cm^2 V^{-1} s^{-1} and in the output current (I_D) to ∼5.8 μA (Figure S7c,d in the SI), highlighting the passivation effect of DMF on the polyphenylsilane NW shell. A shift of the threshold voltage to the positive was also observed (Figure S7c in the SI) after the stability test in ambient air, from V_{th} = −9 to −6 V, verifying passivation of the NW interface and reduction/elimination of the number of occupied traps, which cause screening of the gate electric field. On the basis of a statistical analysis of 10 samples, an increase in the device mobility (μ) was also observed (Figure S8 in the SI). DMA- and *N*-methylformamide (NMF)-treated Si NWs were also investigated, with DMA demonstrating results similar to those of DMF, but their surface analysis needs further investigation. Also, DMF-treated CVD-grown Si NWs showed results similar to those of DMF-treated SFLS-grown Si NWs, with less than 2 V hysteresis in a N_2 environment and less than 1 V when exposed to ambient conditions, further demonstrating passivation effects of DMF for different types of NWs.

As a final step, we have fabricated bottom-gated Si NW FETs on plastic substrates (Kapton) to investigate the compatibility of DMF passivation for plastic electronic devices. The NW FETs with a parylene N gate insulator and DMF-processed NWs demonstrated hysteresis values (∼2.5 V; Figure S9 in the SI) similar to those of the transistors with a SiO_2 dielectric. DMF did not seem to affect the organic gate dielectric or the substrate.

In summary, we have experimentally demonstrated the effect of a DMF solution acting as a mild oxidizing agent and passivation of Si NW shells, resulting in a drastically suppressed NW FET hysteresis. This chemical method can be conducted at room temperature, compatible with the fabrication of NW electronic devices on various substrates including plastics. Bottom-gated FET devices fabricated with Si NWs dispersed in DMF exhibited low hysteresis, on average ∼8 times lower as opposed to using anisole as a dispersant. A hysteresis reduction of over 300 times (from 32 to 0.1 V) was demonstrated with near-zero hysteresis devices obtained with DMF-treated SFLS Si NWs.

DMF-treated NWs exhibited a 1−2 order of magnitude trap density decrease compared to anisole-treated NWs and an increase in the device mobility. DMF-treated devices showed environmental stability, with a further decrease of the hysteresis even after 1000 h of exposure as opposed to the anisole-treated devices. However, a sharp increase in hysteresis was observed for anisole-processed NW FETs after exposure to air.

On the basis of the XPS data, a significant 35% increase of the SiO_2 composition of the NW shell around the core is demonstrated after DMF treatment, passivating the silicon core. The dramatic reduction of hysteresis following the DMF processing indicates that the modified NW shell prevents the adsorption of water molecules on the surface of the silicon core, which is the main source of hysteresis. The shell passivation of Si NWs with DMF considerably improves the fabrication of reliable and reproducible Si NW devices demonstrated with FETs, suitable for printed nanomaterial electronic applications. The NW passivation approach can be extended to other NW applications including supercapacitors, photovoltaics, and photodiodes.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.5b07140.

Experimental section for NW FET device fabrication, XPS sample preparation, NW hysteresis measurements and characterization, FET electrical and trap density characterization, XPS spectral analysis, and NW device mobility statistical analysis (PDF)

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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